What is claimed is:

1. A method for forming gate oxides on a substrate, comprising:

forming a pair of gate oxides to a first thickness on the substrate;

forming a thin dielectric layer on one of the pair of gate oxides, wherein the thin dielectric layer exhibits a high resistance to oxidation at high temperatures; and

forming the other of the pair of gate oxides to a second thickness.

2. The method of claim 1, wherein forming the pair of gate oxides to a first thickness includes forming the pair of gate oxides to a thickness of less than 5 nanometers.

3. The method of claim 1, wherein forming the pair of gate oxides to a first thickness includes using a low-temperature oxidation method.

4. The method of claim 1, wherein forming the pair of gate oxides to a first thickness includes forming the pair of gate oxides by atomic oxygen generated in high-density krypton plasma at approximately 400 degrees Celsius.

5. The method of claim 1, wherein forming a thin dielectric layer (of less than 5 nanometers) on one of the pair of gate oxides includes forming a thin dielectric layer of silicon nitride (Si_3N_4) using jet vapor deposition (JVD).

6. A method for forming gate oxides on a substrate, comprising:

forming a pair of gate oxides to a first thickness on the substrate;

forming a thin dielectric layer on one of the pair of gate oxides, wherein the thin dielectric layer exhibits a high resistance to boron penetration at high temperatures; and

forming the other of the pair of gate oxides to a second thickness.

7. The method of claim 6, wherein forming the pair of gate oxides to a first thickness includes forming the pair of gate oxides to a thickness of less than 5 nanometers by atomic oxygen generated in high-density krypton plasma at approximately 400 degrees Celsius.

8. The method of claim 6, wherein forming a thin dielectric layer on one of the pair of gate oxides includes forming a thin dielectric layer of silicon nitride (Si_3N_4) to a thickness of less than 3 nanometers using jet vapor deposition (JVD).

9. The method of claim 6, wherein forming a thin dielectric layer on one of the pari of gate oxides includes forming a thin dielectric layer which exhibits a strong resistance to the formation of an interfacial oxide layer when forming the other of the pair of gate oxides to a second thickness.

10. The method of claim 6, wherein forming the other of the pair of gate oxides to a second thickness includes forming the other of the pair of gate oxides to a second thickness of less than 10 nanometers by atomic oxygen generated in high-density krypton plasma at approximately 400 degrees Celsius.

11. A method for forming gate oxides on a substrate, comprising:

forming a pair of gate oxides to a first thickness on the substrate;

forming a thin masking layer on one of the pair of gate oxides having a first thickness, wherein the thin masking layer exhibits a high resistance to oxidation at high temperatures; and

[illegible] to a second thickness

12. The method of claim 11, wherein forming the pair of gate oxides to a first thickness includes forming the pair of gate oxides to a thickness of less than 5 nanometers using a low-temperature oxidation method.

13. The method of claim 12, wherein using a low-temperature oxidation method includes forming the pair of gate oxides by atomic oxygen generated in high-density krypton plasma at approximately 400 degrees Celsius.

14. The method of claim 13, wherein forming the other of the pair of gate oxides to a second thickness includes forming the other of the pair of gate oxides to a second thickness of less than 10 nanometers by atomic oxygen generated in high-density krypton plasma at approximately 400 degrees Celsius.

15. The method of claim 11, wherein forming a thin masking layer on one of the pair of gate oxides, wherein the thin masking layer exhibits a high resistance to oxidation at high temperatures includes forming a thin masking layer of silicon nitride (Si_3N_4) to a thickness of less than 3 nanometers using jet vapor deposition (JVD).

16. A method for fabricating a circuit having logic and memory devices on a single substrate, comprising:

forming a number of transistors on the substrate, wherein forming the number of transistors includes forming a first transistor for use in the logic device and forming a second transistor for use in the memory device on the substrate, and wherein forming the first transistor and the second transistor includes:

forming a pair of gate oxides to a first thickness on the substrate;

forming a thin dielectric layer on one of the pair of gate oxides, wherein the thin dielectric layer exhibits a high resistance to

forming the other of the pair of gate oxides to a second thickness; and

wiring the logic device and the memory device together using a metallization process to implement a specific circuit function.

17. The method of claim 16, wherein forming the pair of gate oxides to a first thickness includes a first thickness suitable for the operation of the logic device.

18. The method of claim 16, wherein forming the pair of gate oxides to a first thickness includes forming the pair of gate oxides to a thickness of less than 5 nanometers (nm) by atomic oxygen generated in high-density krypton plasma at approximately 400 degrees Celsius.

19. The method of claim 16, wherein forming a thin dielectric layer on one of the pair of gate oxides includes forming a thin dielectric layer of silicon nitride (Si_3N_4) to a thickness of less than 3 nanometers (nm) using jet vapor deposition (JVD) for use in the logic device.

20. A method for fabricating a circuit having logic and memory devices on a single substrate, comprising:

forming a number of transistors on the substrate, wherein forming the number of transistors includes forming at least one transistor for use in the logic device and forming at least one transistor for use in the memory device on the substrate, and wherein forming the first and the second transistors includes;

forming a pair of gate oxides to a first thickness suitable for the operation of the logic device on the substrate;

forming a thin dielectric layer on one of the pair of gate oxides, wherein the thin dielectric layer exhibits a high resistance to boron penetration at high temperatures; and

[illegible] to a second thickness; and

wiring the logic device to the memory device using a metallization process to implement a specific circuit function.

21. The method of claim 20, wherein forming the pair of gate oxides to a first

thickness includes forming the pair of gate oxides to a thickness of less than 5 nanometers by a process using atomic oxygen generated in high-density krypton plasma at approximately 400 degrees Celsius.

22. The method of claim 20, wherein forming a thin dielectric layer on one of the pair of gate oxides includes forming a thin dielectric layer of silicon nitride (Si_3N_4) to a thickness of less than 3 nanometers using jet vapor deposition (JVD) for use in the logic device.

23. The method of claim 22, wherein forming a thin dielectric layer on one of the pair of gate oxides for use in the logic device is performed before forming the other of the pair of gate oxides to a second thickness.

24. The method of claim 20, wherein forming a thin dielectric layer on one of the pair of gate oxides includes forming a thin dielectric layer which exhibits a strong resistance to the formation of an interfacial oxide layer when forming the other of the pair of gate oxides to a second thickness.

25. The method of claim 24, wherein forming the other of the pair of gate oxides to a second thickness includes forming the other of the pair of gate oxides to a second thickness of less than 10 nanometers including the first thickness, which has not been etched, by a process using atomic oxygen generated in high-density krypton plasma at approximately 400 degrees Celsius for use in the memory device.

26. The method of claim 25, wherein the method of forming the first and the second transistors further includes forming a boron doped polysilicon gate on the thin dielectric layer as part of the first transistor and on the other gate oxide as part of the second transistor.

27. A method for fabricating a circuit having logic and memory devices on a single substrate, comprising:

forming a number of transistors on the substrate, wherein forming the number of transistors includes forming at least one transistor for use in a logic device and forming at least one transistor for use in a memory device on the substrate, and wherein forming the first transistor and the second transistor includes;

forming a pair of gate oxides to a first thickness on the substrate;

forming a thin layer of silicon nitride (Si_3N_4) on one of the pair of gate oxides using jet vapor deposition (JVD); and

forming the other of the pair of gate oxides to a second thickness; and;

wiring the logic device to the memory device using a metallization process to implement a specific circuit function.

28. The method of claim 27, wherein forming the pair of gate oxides to a first thickness includes forming the pair of gate oxides to a thickness of suitable for use in the logic device using a low-temperature oxidation method.

29. The method of claim 28, wherein forming the pair of gate oxides to a first thickness of suitable for use in the logic device includes forming the pair of gate oxides to a first thickness of less than 5 nanometers.

30. The method of claim 29, wherein forming the pair of gate oxides to a first [illegible] method includes forming the pair of gate oxides by a process using atomic oxygen generated in high-density krypton plasma at approximately 400 degrees Celsius.

31. The method of claim 27, wherein forming a thin layer of silicon nitride (Si_3N_4) on one of the pair of gate oxides using jet vapor deposition (JVD) includes

forming a thin layer of silicon nitride (Si_3N_4) on one of the pair of gate oxides for use in the logic device.

32. The method of claim 31, wherein forming a thin layer of silicon nitride (Si_3N_4) on one of the pair of gate oxides for use in the logic device includes forming the thin layer of Si_3N_4 to have a thickness of less than 3 nanometers.

33. A logic device and a memory device structure on a single substrate, comprising:

a first transistor having a source and a drain region in the substrate separated by a channel region in the substrate, wherein the first transistor includes a dielectric layer of a first thickness, including a top layer which exhibits a high resistance to oxidation at high temperatures, separating a gate from the channel region; and

a second transistor having a source and a drain region in the substrate separated by a channel region in the substrate, wherein the second transistor includes a dielectric layer of second thickness separating a gate from the channel region.

34. The structure of claim 33, wherein the first transistor is a transistor for the logic device and the second transistor is a transistor for the memory device.

35. The structure of claim 33, wherein the first transistor having a dielectric layer of a first thickness includes a dielectric layer having a thickness of less than 7

36. The structure of claim 33, wherein the first transistor having a dielectric layer of a first thickness includes a bottom layer of silicon dioxide (SiO_2) and a top layer of silicon nitride (Si_3N_4).

37. The structure of claim 33, wherein the second transistor having a dielectric layer of second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

38. The structure of claim 33, wherein the second transistor having a dielectric layer of second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

39. The structure of claim 33, wherein the first transistor which includes a dielectric layer of a first thickness and having a top layer which exhibits a high resistance to oxidation at high temperatures includes a top layer of silicon nitride (Si_3N_4) which comprises approximately a third of the first thickness of the dielectric layer.

40. The structure of claim 33, wherein the first transistor which includes a dielectric layer of a first thickness includes a dielectric layer having a thickness of less than 7 nanometers, wherein the dielectric layer has a bottom layer of silicon dioxide (SiO_2), and wherein the top layer is silicon nitride (Si_3N_4).

41. A circuit on a single substrate, comprising:

a logic device, wherein the logic device further includes a transistor with a dielectric layer having a first thickness including a top layer which exhibits a high resistance to oxidation at high temperatures; and

a memory device coupled to the logic device, wherein the memory device further [illegible]

greater than the dielectric layer of the first thickness but less than 12 nanometers, wherein the dielectric layer of the second thickness is formed entirely of silicon dioxide (SiO_2).

42. The circuit of claim 41, wherein the dielectric layer having a first thickness

includes a dielectric layer of less than 7 nanometers, wherein the dielectric layer has a bottom layer of silicon dioxide (SiO_2), and wherein the top layer is silicon nitride (Si_3N_4).

43. The circuit of claim 41, wherein the logic device transistor and the memory device transistor both include a gate formed from boron doped polysilicon, and wherein the top layer of the dielectric layer having a first thickness exhibits a strong resistance to boron penetration at high temperatures.

44. The circuit of claim 43, wherein the top layer of the dielectric layer having a first thickness exhibits a strong resistance to boron penetration at temperatures above approximately 300 degrees Celsius.

45. The circuit of claim 41, wherein the dielectric layer of a first thickness having a top layer which exhibits a high resistance to oxidation at high temperatures includes a top layer of silicon nitride (Si_3N_4) which comprises approximately a third of the first thickness of the dielectric layer.

46. The circuit of claim 45, wherein the top layer of the dielectric layer of the first thickness has a thickness of less than 2 nanometers.

47. A system on a chip, comprising:

a logic device, wherein the logic device further includes a transistor with a dielectric layer having a first thickness of less than 7 nanometers including a top

a memory device coupled to the logic device, wherein the memory device further includes a transistor with a dielectric layer having a second thickness greater than the dielectric layer of the first thickness but less than 12 nanometers.

48. The system of claim 47, wherein the dielectric layer having a first thickness

includes a dielectric layer having a bottom layer of silicon dioxide (SiO_2), and wherein the top layer is silicon nitride (Si_3N_4).

49. The system of claim 47, wherein the logic device transistor and the memory device transistor both include a gate formed from boron doped polysilicon, and wherein the top layer of the dielectric layer having a first thickness exhibits a strong resistance to boron penetration at high temperatures.

50. The system of claim 49, wherein the top layer of the dielectric layer having a first thickness exhibits a strong resistance to boron penetration at temperatures above approximately 300 degrees Celsius.

51. The system of claim 49, wherein the top layer of the dielectric layer having a first thickness exhibits a strong resistance to boron penetration at temperatures above approximately 800 degrees Celsius.

52. The system of claim 47, wherein the dielectric layer of a first thickness having a top layer which exhibits a high resistance to oxidation at high temperatures includes a top layer of silicon nitride (Si_3N_4) which comprises approximately a third of the first thickness of the dielectric layer.

53. The circuit of claim 52, wherein the top layer of the dielectric layer of the first thickness has a thickness of less than 2 nanometers.

[illegible] the dielectric layer of the second thickness is formed entirely of silicon dioxide (SiO_2)